DOCKET NO.: RMK-2003-0025-US1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Robert M. Geffken	EXAMINER:	Nguyen, D. H.
SERIAL NO.:	10/605,440	ART UNIT:	2818
FILING DATE:	September 30, 2003	DATE:	July 28, 2005
FOR:	Adjustable Self-Aligned Air Gap Dielectric for Low Capacitance Wiring		

DECLARATION UNDER RULE 131

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

We, Robert M. Geffken and William T. Motsiff, do hereby declare as follows:

1. We were formerly employees of International Business Machines Corporation ("IBM"), the assignee of the above-identified patent application entitled "Adjustable Self-Aligned Air Gap Dielectric for Low Capacitance Wiring." We are co-inventors of the invention described and claimed in the above-identified application.

2. This is a declaration under the provisions of 37 CFR § 1.131 for the purpose of swearing back of references which were cited in the subject application. This declaration establishes facts showing conception of this invention in this country prior to the November 15, 2002 filing date of Lur et al. U.S. Patent Publication No. US

2004/0097065 A1 and the December 20, 2002 filing date of Goldberg et al. U.S. Patent No. 6,838,354 cited against this application, and due diligence from a time prior to the former date until the application was filed.

3. The claimed invention in the above-identified application was conceived by us in the United States prior to November 15, 2002. This is evidenced by the appended copy of a portion of an invention disclosure form created by Robert Geffken on our behalf describing the invention disclosed in the subject patent application (the "Disclosure"), attached hereto as Exhibit A. The Exhibit A Disclosure references drawings in two electronic documents created by us, SelfalignedAirgap1.prz (the "First Embodiment"), attached as Exhibit B, and SelfalignedAirgap2.prz (the "Second Embodiment"), attached as Exhibit C. Encircled page numbers have been added to the First and Second Embodiments to assist in identifying relevant disclosure.

4. Although the copy of the Exhibit A Disclosure is indicated as being printed on April 12, 2003, the relevant portions of the Disclosure were in fact created, and the Disclosure is dated as being created, prior to November 15, 2002, the filing date of the Lur et al. patent publication. The First and Second Embodiments in Exhibits B and C are undated, but were created by us prior to November 15, 2002. Actual dates prior to November 15, 2002 and material not pertinent to conception of the invention have been redacted in view of their confidential nature.

5. The invention claimed in the subject application is directed to a semiconductor device having an air gap formed between first and second interconnects.

The following chart compares the steps of the claimed semiconductor device with the teachings in the Disclosure and First and Second Embodiments of Exhibits A, B and C:

CLAIM 1	DISCLOSURE
A semiconductor device comprising:	"Adjustable, Self Aligned Airgap Dielectric for Low Capacitance Wiring." Disclosure, page 1. "Self Aligned Airgap Insulator with Adjustable height." First and Second Embodiments, page 1.
a first interconnect adjacent a second interconnect on an interconnect level;	"Standard Barrier-Seed layer and Cu deposition processes are used to fill the dual damascene structure ... ." Disclosure, page 3. "Liner/Seed layer, Cu Deposition." First and Second Embodiments, page 6 (upper drawing). Spaced, adjacent first and second interconnects on the same interconnect level. First and Second Embodiments, page 6 (lower drawing) and page 7 (both drawings).
spacers formed along adjacent sides of the first and second interconnects; and	"[C]onformal deposition of a second insulator eg SiO2 or Si3N4 is applied to the existing structure. A second spacer etch is now done and the bottom capping layer is also opened. Disclosure, page 3. "Conformal Insulator Deposition eg. SiO2" and "Oxide Spacer Etch & Cap Open." First and Second Embodiments, page 5. Spacers shown along adjacent sides of the first and second interconnects. First and Second Embodiments, pages 6 and 7.

an air gap formed between the first and second interconnects, the air gap extending above an upper surface of at least one of the first and second interconnects and below a lower surface of at least one of the first and second interconnects, distance between the spacers defining the width of the air gap.

"A resist blockmask is used to expose only those areas which will receive the airgap. The SiC, SiCOH, SiC exposed layers are degrades by exposure to oxygen plasma followed by dilute HF etch which creates a space with an overhang between unmasked minimum space lines. Nitride cap layer and FSG conformal deposition processes are now done which close the airgap layer." Disclosure, page 3.
"Etch SiC HM1, Extract Low k & Etch SiC in Min. Space Areas" and "Conformal Insulator Deposition – Nitride Cap & FSG to form Airgap." Air gap shown as formed between the first and second interconnects, with the air gap extending above the upper surface of both interconnects and below the lower surface of the left interconnect, and with the air gap width defined by the distance between the spacers. First and Second Embodiments, page 7.

6. The Disclosure and First and Second Embodiments of Exhibits A, B and C were submitted for internal review by the invention disclosure team and patent agents and attorneys at IBM prior to November 15, 2002.

7. On December 3, 2002, Mr. Motsiff provided to Anthony Canale, the IBM patent agent responsible for the subject patent application, additional information concerning the disclosure of the subject invention.

8. Subsequently, the subject invention as disclosed in the Disclosure and First and Second Embodiments of Exhibits A, B and C, as well as the additional information provided on December 3, 2002 was reviewed by Anthony Canale, and a decision was made to file a patent application on the invention.

9. On April 14, 2003, the Disclosure and First and Second Embodiments of Exhibits A, B and C, as well as the additional information provided on December 3, 2002 was sent to Attorney Peter Peterson of DeLio & Peterson LLC, New Haven, Connecticut, the outside counsel who was responsible for preparing the application.

10. On June 30 and July 7, 2003, Mr. Motsiff received drafts of the subject patent application for the claimed invention by facsimile from Atty. Peterson, including informal drawings and a partial set of claims. Mr. Geffken at that time was retired from IBM, so that there was some delay in communication between us concerning the draft application. Also, at the time of late June to early July, 2003, Mr. Motsiff was away from his office at IBM.

11. On July 21, 2003, Mr. Motsiff emailed to Atty. Peterson a communication that acknowledged receipt of the fax copy of the draft patent application and requested an electronic (soft) copy of the application for annotation.

12. On August 11, 2003, Mr. Motsiff faxed to Atty. Peterson revisions to the draft patent application, including revisions to the specification and drawings.

13. On August 19, 2003, Mr. Motsiff emailed to Atty. Peterson revisions to the claims of the draft application.

14. On August 21, 2003, Mr. Motsiff received by fax from Atty. Peterson a revised draft of the subject application.

15. On September 2, 2003, Mr. Motsiff received by fax from Atty. Peterson revised informal drawings for the subject application. Subsequently, we reviewed the

revised application and drawings, and communicated to Atty. Peterson that the subject application was ready for filing.

16. We are informed that on or about September 3, 2003, Mr. Peterson ordered formal drawings for the subject patent application, and that those drawings were sent to IBM on or about September 25, 2003.

17. On September 29, 2003, we reviewed the final version of the subject patent application and executed the declaration for the application.

18. On September 30, 2003, the subject application was filed with the U.S. Patent and Trademark Office.

19. We declare further that all statements made on our own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements and the like so made are punishable by fine or imprisonment or both, under §1001 of the Title XVIII of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issuing thereon.

Robert M Geffken — 27 July 2005

Name: Robert M. Geffken — Date

William T. Motsiff — 27 July 2005

Name: William T. Motsiff — Date

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Name: Barbara Browne Date: July 28, 2005 Signature: Barbara Browne

Disclosure BUR8-2002-0129

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Robert Geffken On [redacted]02:05:26 PM EDT
Last Modified By Maura Mulligan On 03/28/2003 10:29:29 PM EST

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
Adjustable, Self Aligned Airgap Dielectric for Low Cacitance Wiring

Summary

Status		Final Decision **(File)**
Final Deadline		
Final Deadline Reason		
Docket Family		BUR9-2003-0025
*Processing Location		Burlington
*Functional Area	select	
Attorney/Patent Professional		Anthony Canale/Burlington/IBM
IDT Team	select	William Motsiff/Burlington/IBM Matt Rutten/Burlington/IBM Tony Stamper/Burlington/IBM Tom McDevitt/Burlington/IBM Henry Trombley/Burlington/IBM Jeffrey Gambino/Fishkill/IBM Erick Walton/Burlington/IBM
Submitted Date		[redacted]01:36:20 PM EDT
*Owning Division	select	MD
Incentive Program		
Lab		Slattery
*Technology Code		1011
PVT Score	33	

Inventors with a Blue Pages entry

Inventors: Robert Geffken/Burlington/IBM, William Motsiff/Burlington/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Geffken, R.M. (Robert)	[redacted]	29/BLBV	446-8613	Miura, Steve S.
Motsiff, W.T. (William)	[redacted]	29/41SA	446-8214	Nye, Henry A. III

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional: Anthony Canale/Burlington/IBM

IDT Team
William Motsiff/Burlington/IBM
Matt Rutten/Burlington/IBM
Tony Stamper/Burlington/IBM
Tom McDevitt/Burlington/IBM
Henry Trombley/Burlington/IBM
Jeffrey Gambino/Fishkill/IBM
Erick Walton/Burlington/IBM

Response Due to IP&L [redacted]

***Main Idea**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

There are a number of interconnect wiring challenges facing the technical community over the next few technology generations.

1) The primary solution being pursued to lower interconnect capacitance is use of "porous dielectrics" These materials have much reduced mechanical strength and thermal conductivity. These result in an increasing challenge to build the chip and dissipate heat during chip operation.

2) In the next few technology generations, the copper resistivity will begin to rise as the wire linewidth starts to approach it's electron mean free path. This resistivity rise is exascerbated by surface & interface roughness. Dual damascene trench & via sidewalls will intersect the low k voids & hasten the Cu resistivity rise.

3) By the 65 nm generation, it is expected that PVD (sputtered) barriers will need to be replaced with CVD or ALD (atomic layer deposition)barriers to meet ongoing thickness reductions and improved conformality requirements. If porous low k is open cell (connected pore) then the CVD or ALD precursors can diffuse into the dielectric and destroy it's k value. Also depending upon the max pore size of the low k material, the thinner liners might not be able to provide continuous coverage to prevent Cu diffusion into the dielectric. For example Porous SILK version 9 still has 200A max pore size when barrier needs to be about 50A in 65 nm node (2007).

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

This invention utilizes a self aligned and adjustable airgap dielectric to reduce capacitance. The height of the airgap above and below the adjacent copper line can be selected to cut off fringing capacitance an increase the effective k of the structure. The via dielectric employed is an oxide (USG or FSG) with relatively good mechanical properties and thermal conductivity. A sacrificial trench dielectric & etchstop layer is used to make the airgap & these may be made of higher thermal conductivity & mechanical strength materials. A block mask is used so that only areas on the chip with minimum spaces and a need for low capacitance receives the airgap. This maximizes the thermal conductance & mechanical stability of the chip.

The trench & via is defined by an oxide or nitride spacer and therefore none of the porous low k issues with the Cu resistivity rise or incompatibility with liner deposition processes are valid.

Two primary embodiments are shown below: In the first embodiment a dielectric stack is deposited over a previously existing copper wiring level.

The stack consists of a cap layer eg. silicon nitride, an insulator with good mechanical properties and thermal conductivity eg FSG, an Etch stop layer (ES1) eg SiC, a low k material with good mechanicals & thermal conductivity eg SiCOH and a first hardmask layer (HM1) eg SiC. An ARC and Resist are applied, imaged for the trench pattern and the hardmask is etched. Next a second hardmask layer (HM2) eg SiO2

or Si3N4 is deposited. The via resist is applied, imaged and the HM2 and the via is etched, The via resist is stripped and then there is a blanket directional removal of HM2 which leaves HM2 spacers adjacent to all areas of HM1 edges except areas exposed by via photo. Note that the size of the spacer is determined by HM1 & HM2 thickness. The trench is now etched down to the ES1 layer.

Next a conformal deposition of a second insulator eg SiO2 or Si3N4 is applied to the existing structure. A second spacer etch is now done and the bottom capping layer is also opened. Note that since this second spacer has reduced the size of the trench and via opening, the initial trench and via photo needs to be exposed & etched larger by 2X the spacer width.

Standard Barrier-Seed layer and Cu deposition processes are used to fill the dual damscene structure and then the excess material is removed by CMP. A resist block mask is used to expose only those areas which will receive the airgap. The SiC, SiCOH, SiC exposed layers are degraded by exposure to oxygen plasma followed by dilute HF etch which creates a space with an overhang between unmasked minimum space lines. Nitride cap layer and FSG conformal deposition processes are now done which close the airgap layer. Alternatively a spin on dielectric may also be used which would be chosen because of it's surface tension properties to leave the airgap unfilled.

The second embodiment below is a similar sequence except that the Si3N4 capping layer is replaced by a self aligned metal capping layer such as selective tungsten.


SelfalignedAirgap1.pi


SelfalignedAirgap2.pi

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
An airgap was proposed by the V Arnal et al, ST Microelectronics but it used a mask to make the airgap & was not self aligned or adjustable.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1-9 must be answered in English)**

***Question 1**
On what date was the invention workable? [redacted] **Please format the date as MM/DD/YYYY**
(Workable means i.e. when you know that your design will solve the problem)

***Question 2**
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?
○ Yes
● No

If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

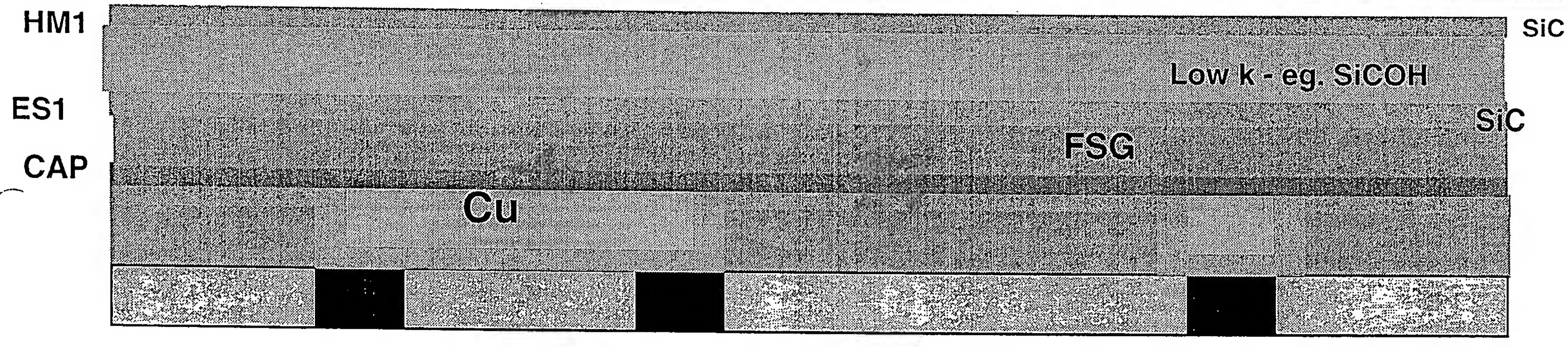
Are you aware of any publications, products or patents that relate to this invention?
● Yes
○ No

If yes, Enter the name of each publication or patent and the date published below.
Publication: "Integration of a 3 Level Cu-SiO2 Air Gap Interconnect for sub 0.1 micron CMOS technologies" V Arnal et al, Proceedings of the 2001 IITC, p 298
Date Published or Issued:

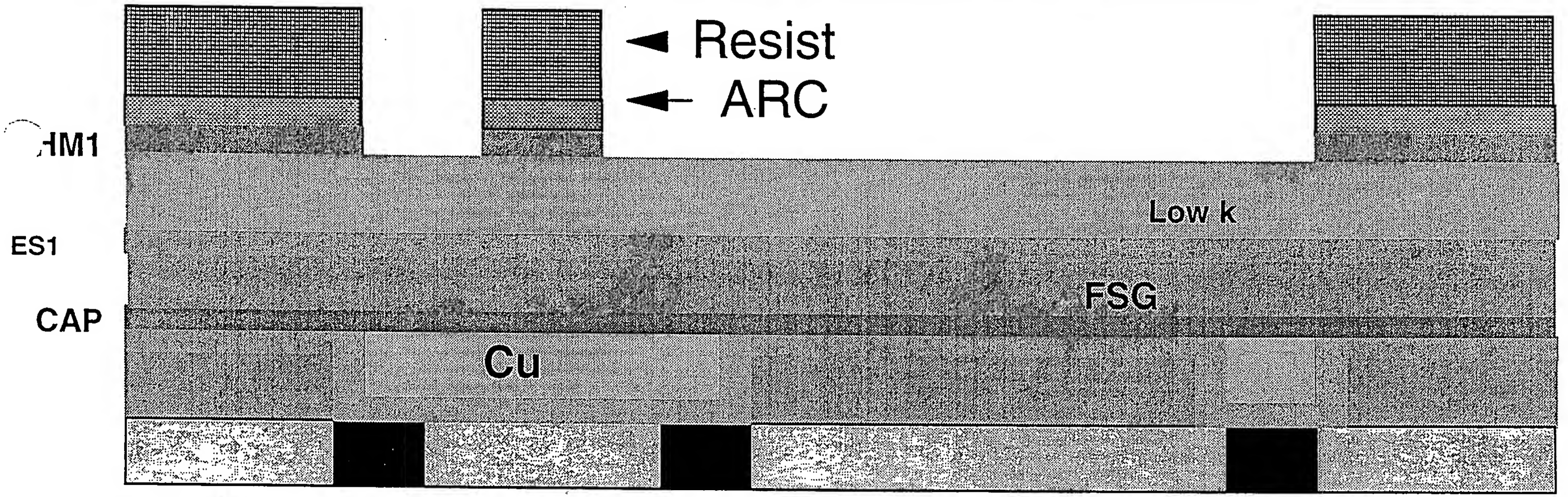
Self Aligned Airgap Insulator with Adjustable height

Embodiment 1

IMD Layer Deposition

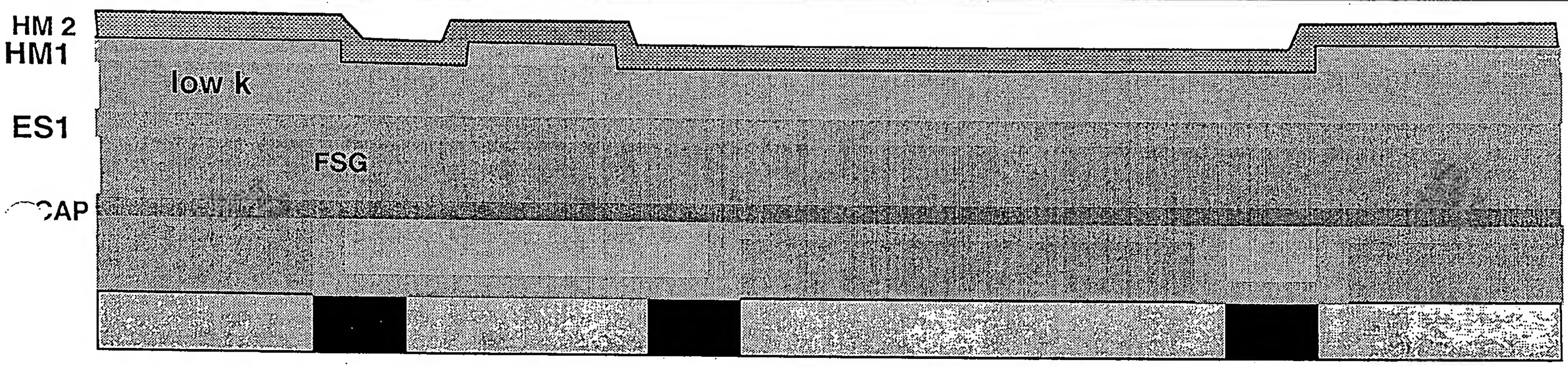


IMD Deposition + Hardmask

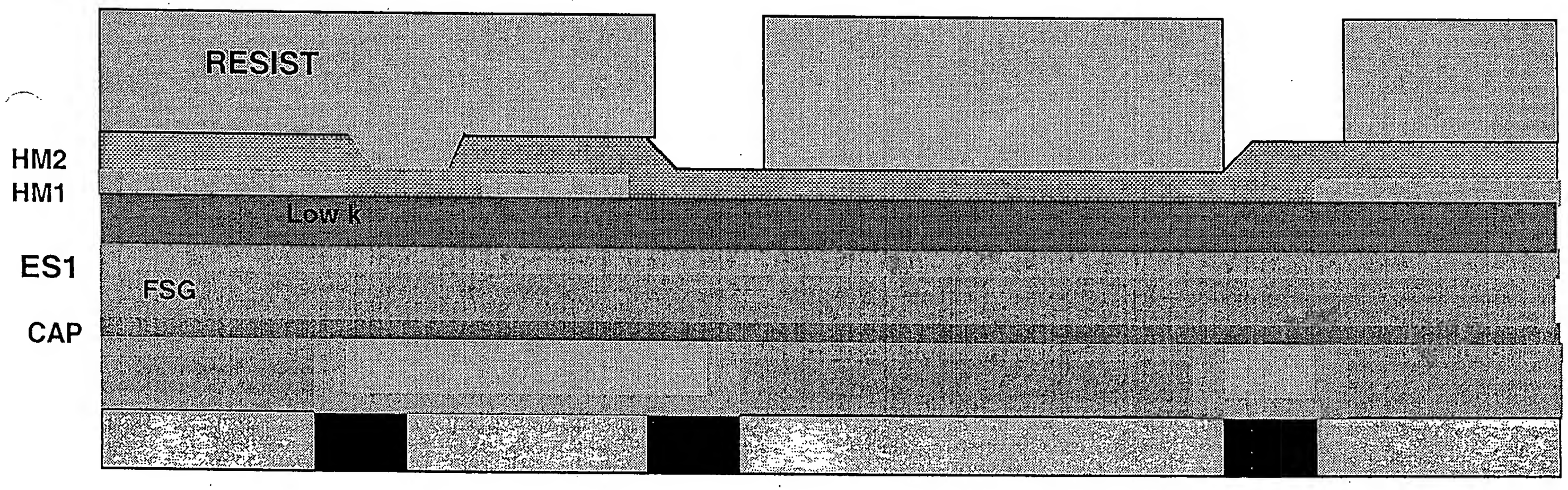


ARC + M2 Resist > Trough Exp. & HM1 RIE

Low k Patterning

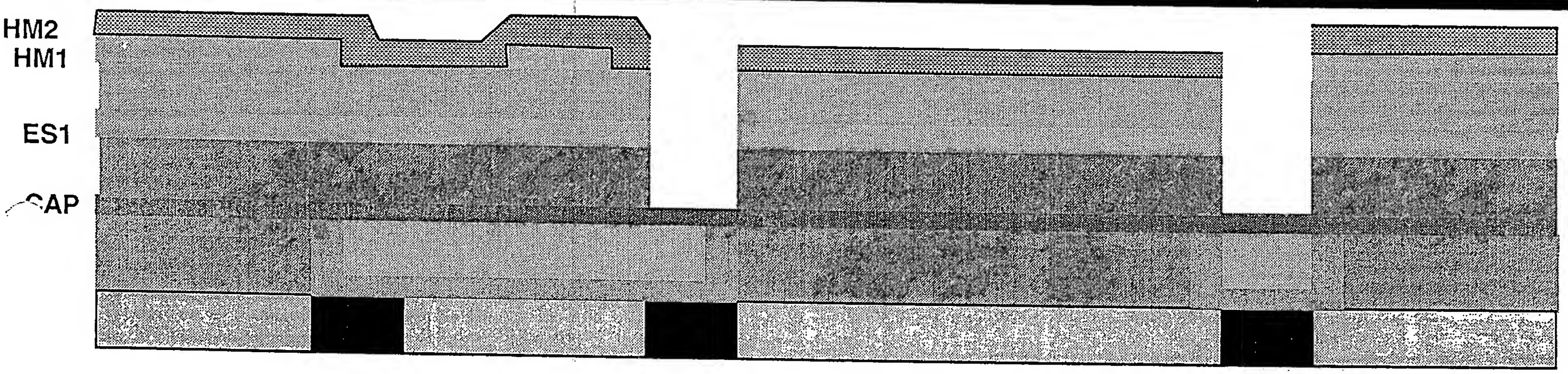


HM2 Deposition

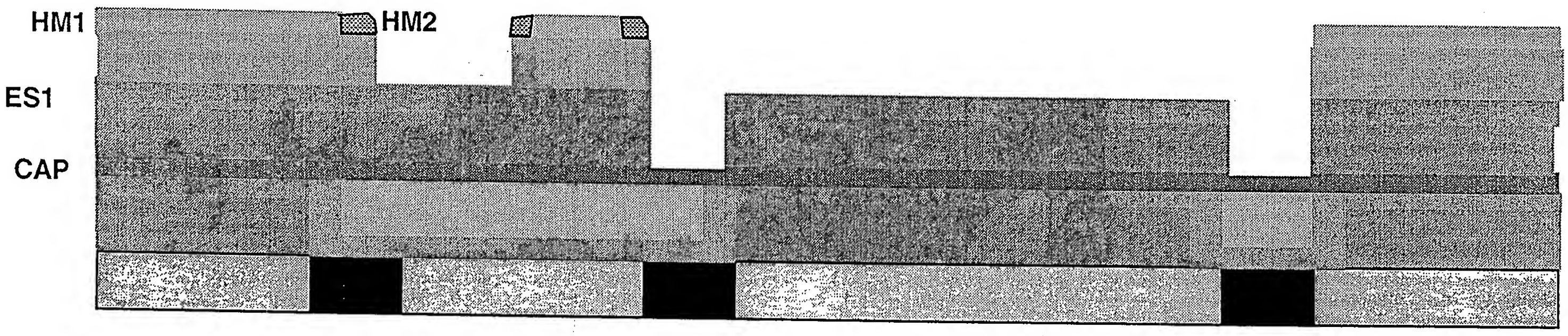


Via resist pattern

Low k Patterning

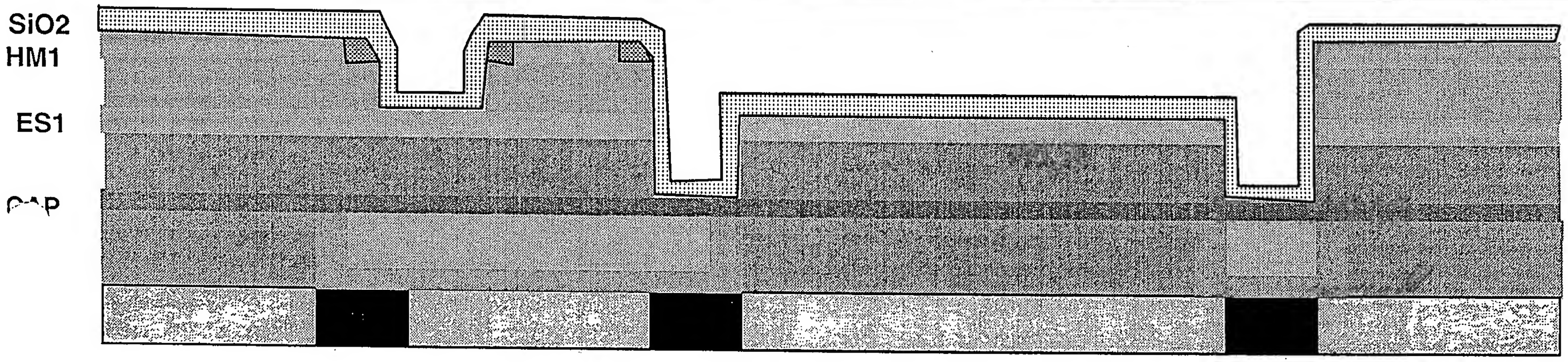


Via Etch & Resist strip

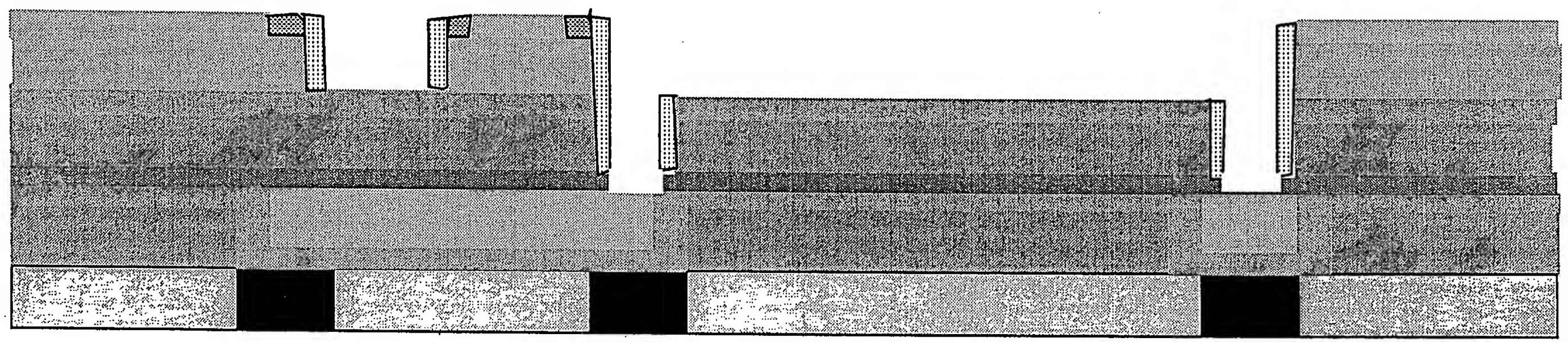


Hardmask 2 Spacer Etch &Trench Etch

Low k Patterning

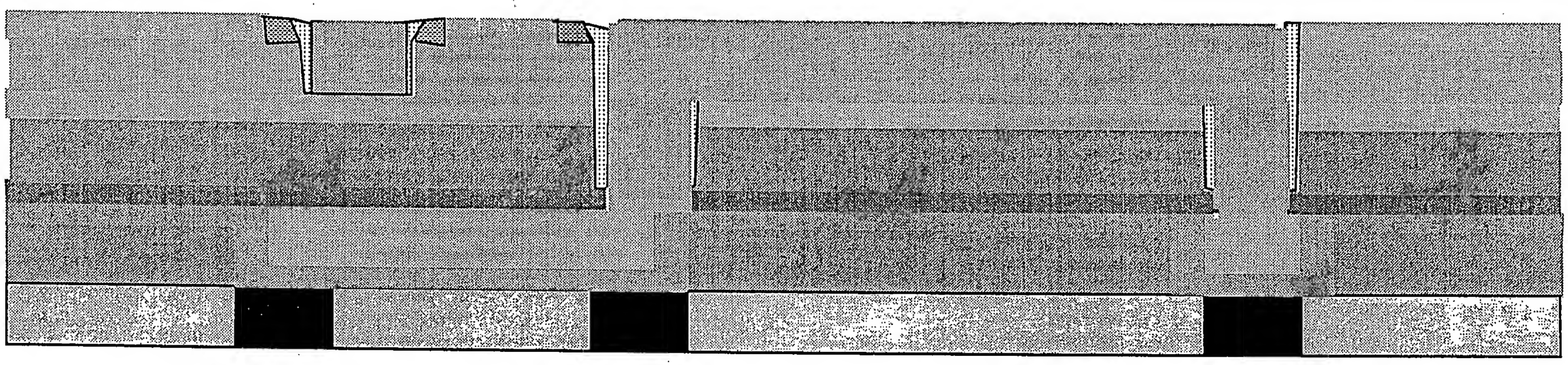


Conformal Insulator Deposition eg. SiO2

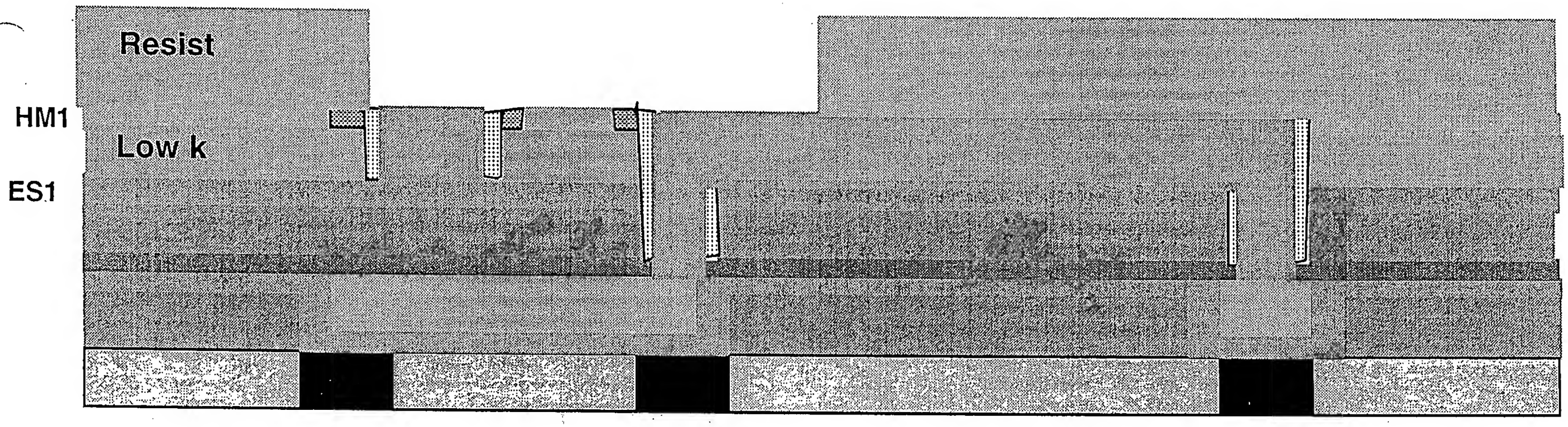


Oxide Spacer Etch & Cap Open

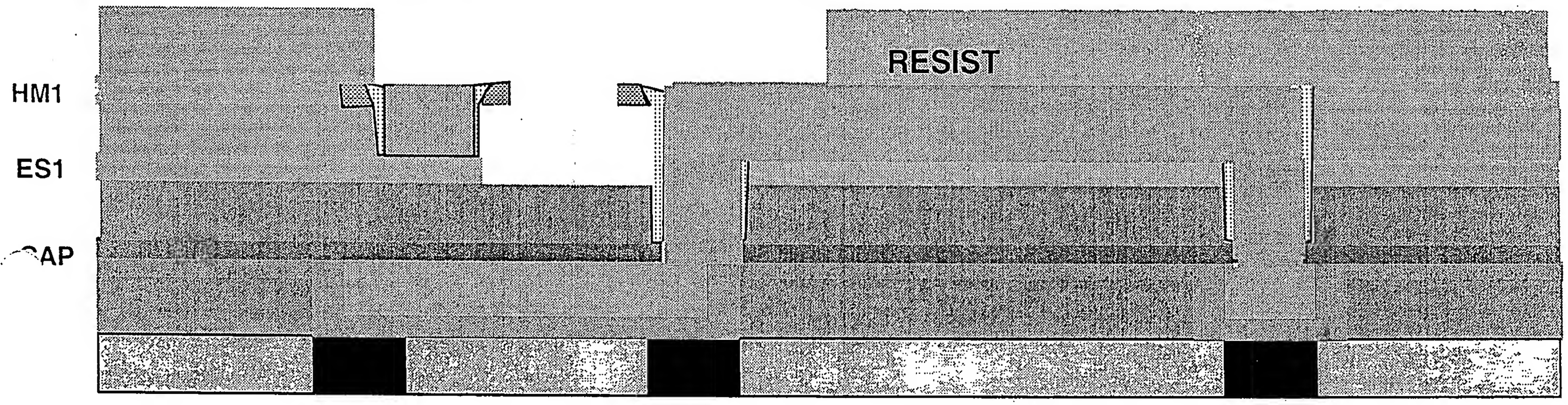
Cu Deposition, CMP & Block Mask



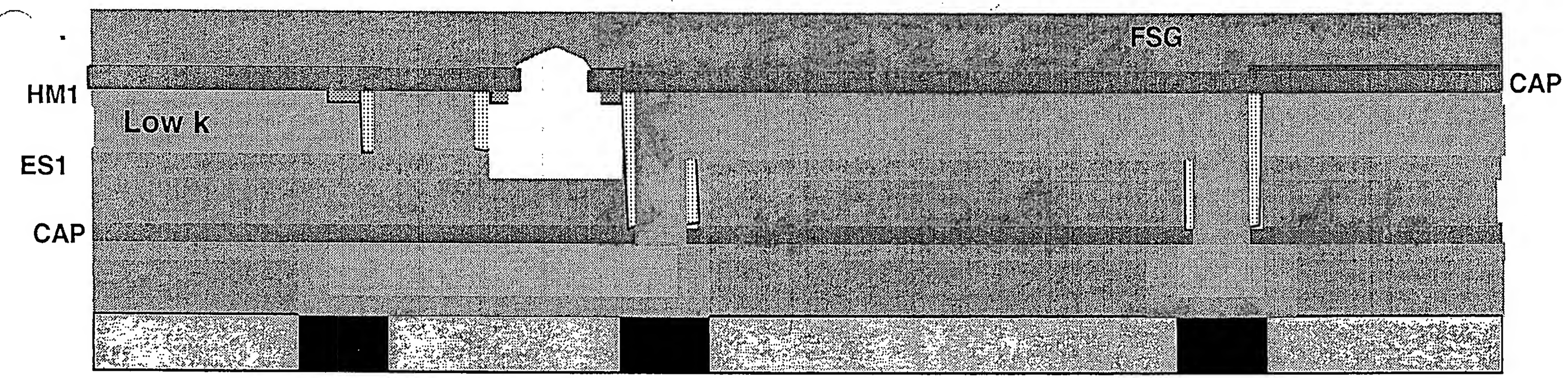
Liner/Seed layer,Cu Deposition- Chem Mech Polish



Resist Block Mask - Expose Min.Space areas



Etch SiC HM1, Extract Low k & Etch SiC in Min.Space Areas

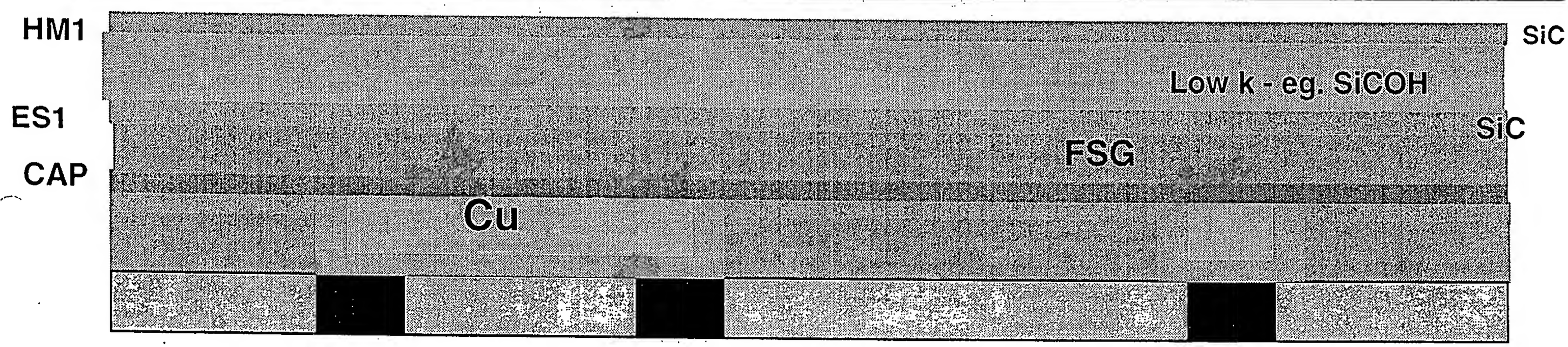


Conformal Insulator Deposition - Nitride Cap & FSG to form Airgap

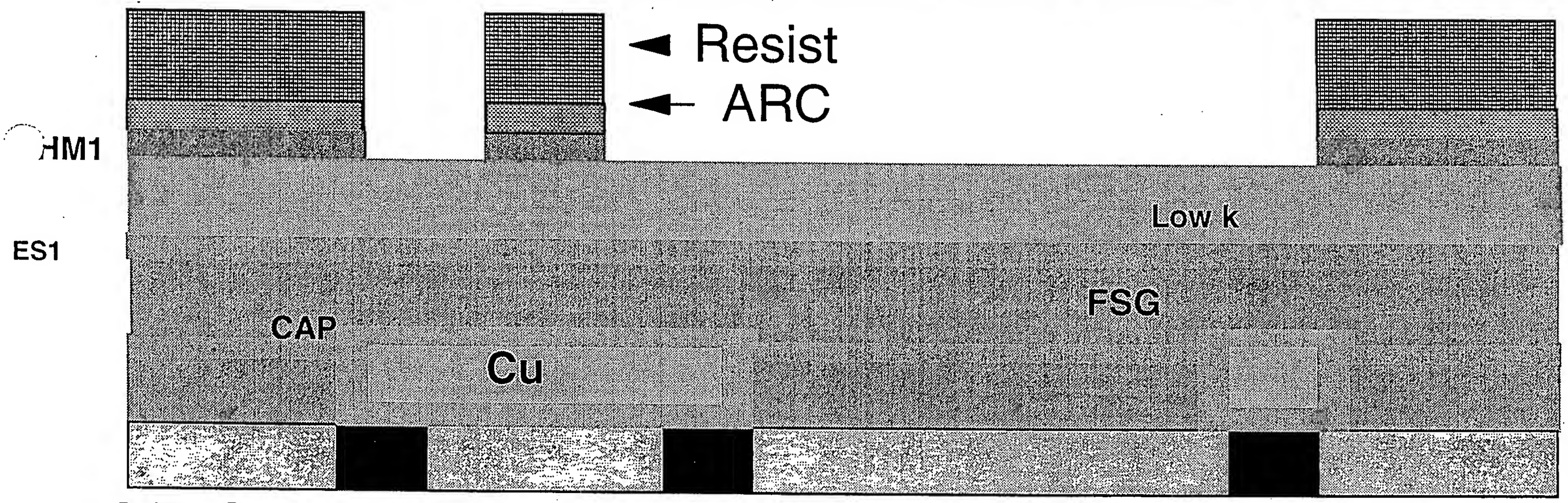
Self Aligned Airgap Insulator with Adjustable height

Embodiment 2

IMD Layer Deposition

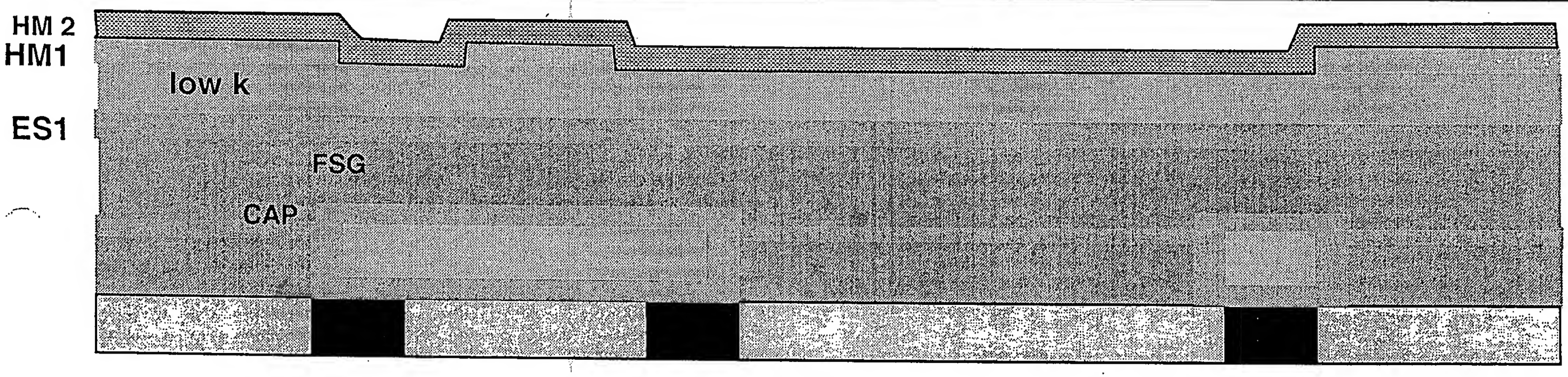


IMD Deposition + Hardmask

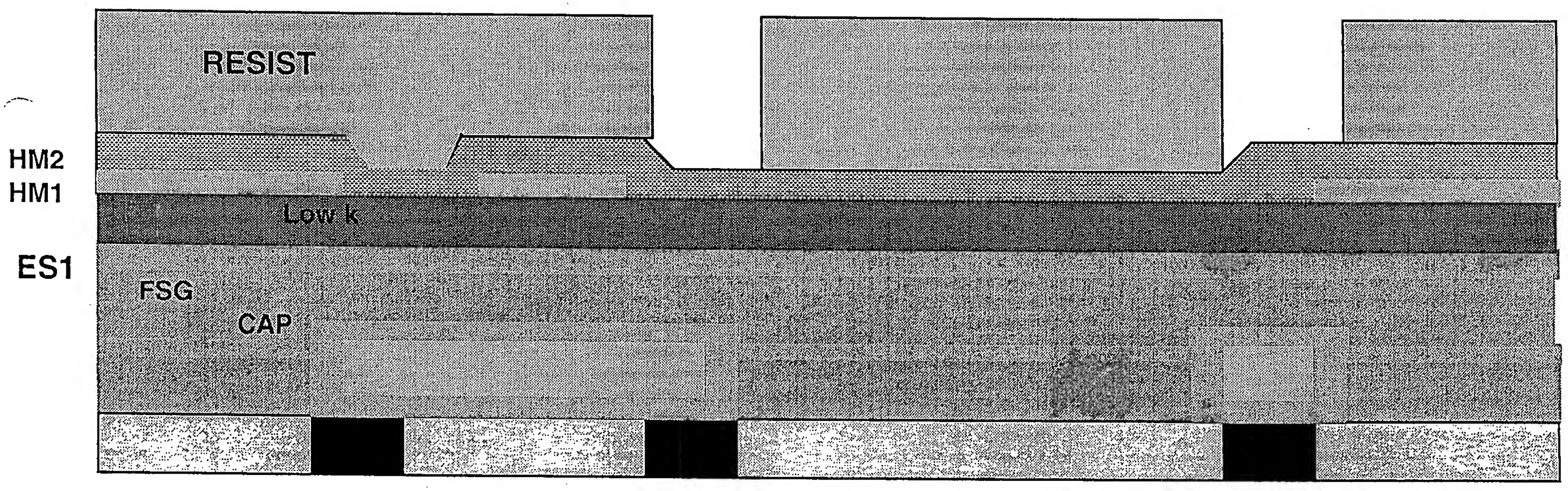


ARC + M2 Resist > Trough Exp. & HM1 RIE

Low k Patterning

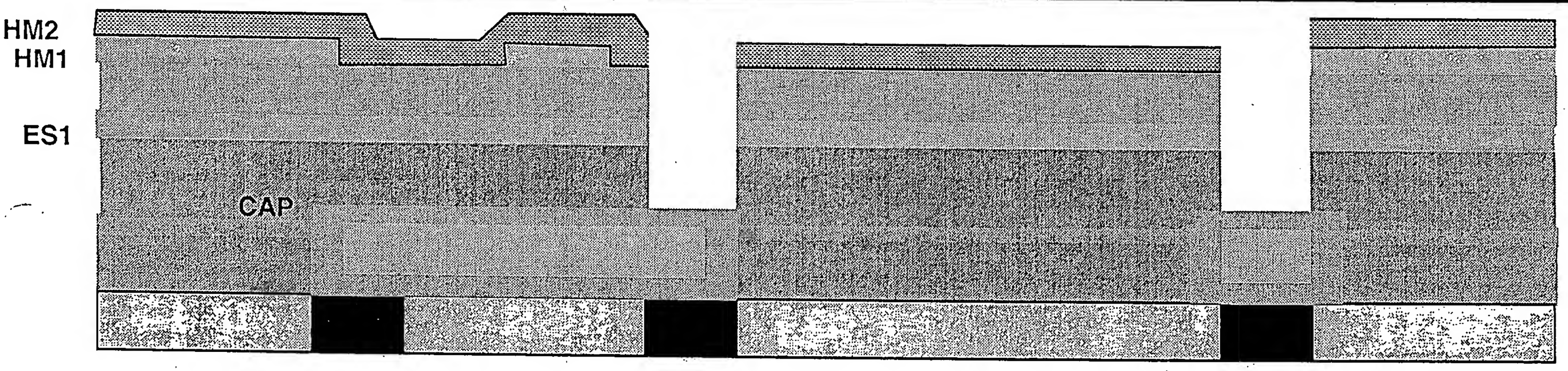


HM2 Deposition

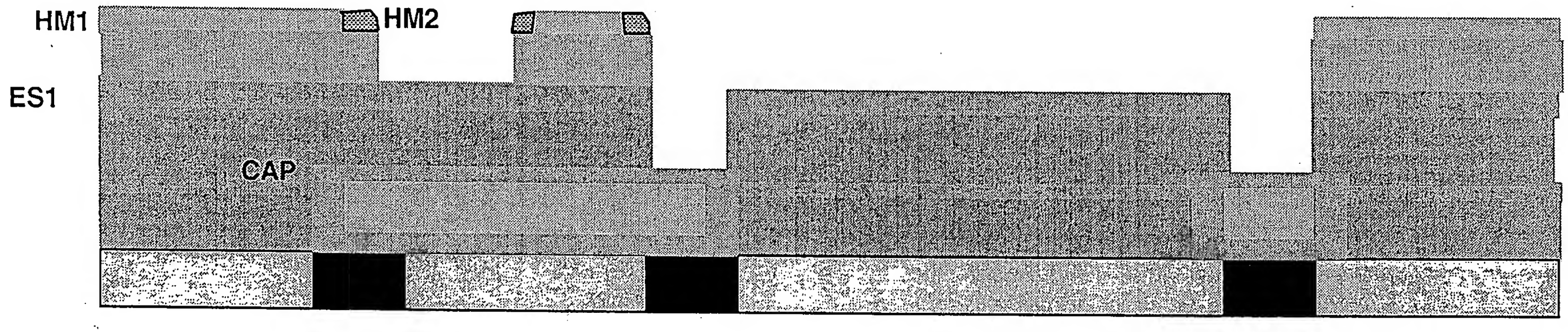


Via resist pattern

Low k Patterning

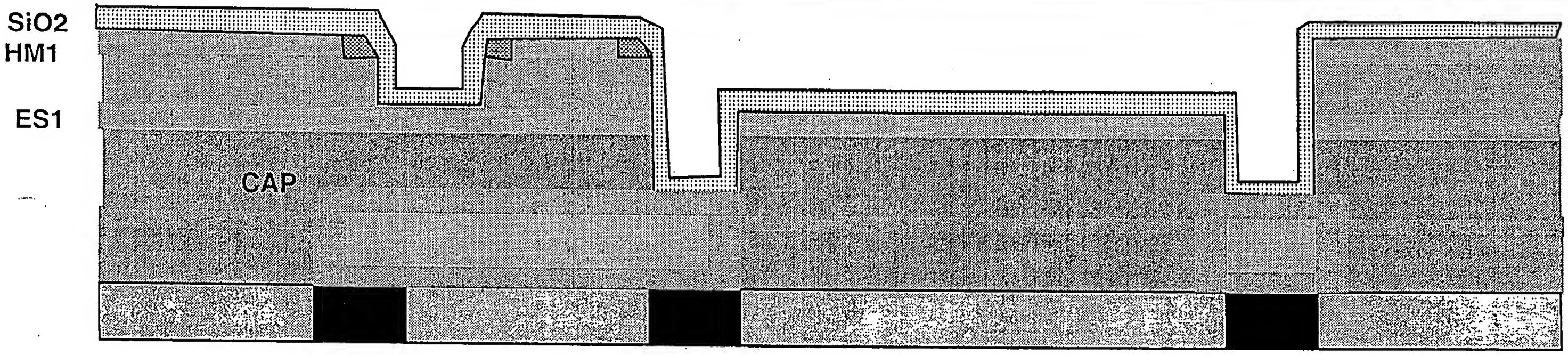


Via Etch & Resist strip

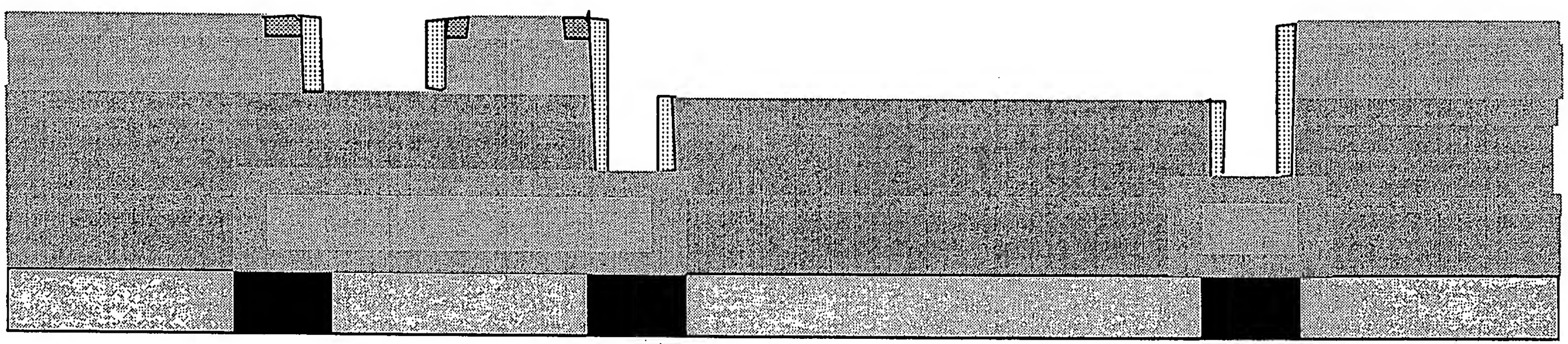


Hardmask 2 Spacer Etch &Trench Etch

Low k Patterning

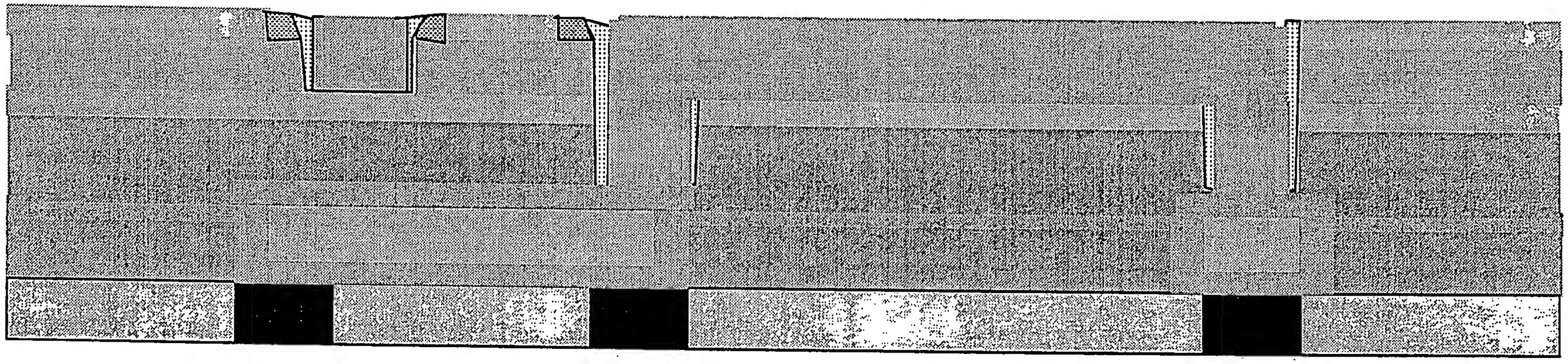


Conformal Insulator Deposition eg. SiO2

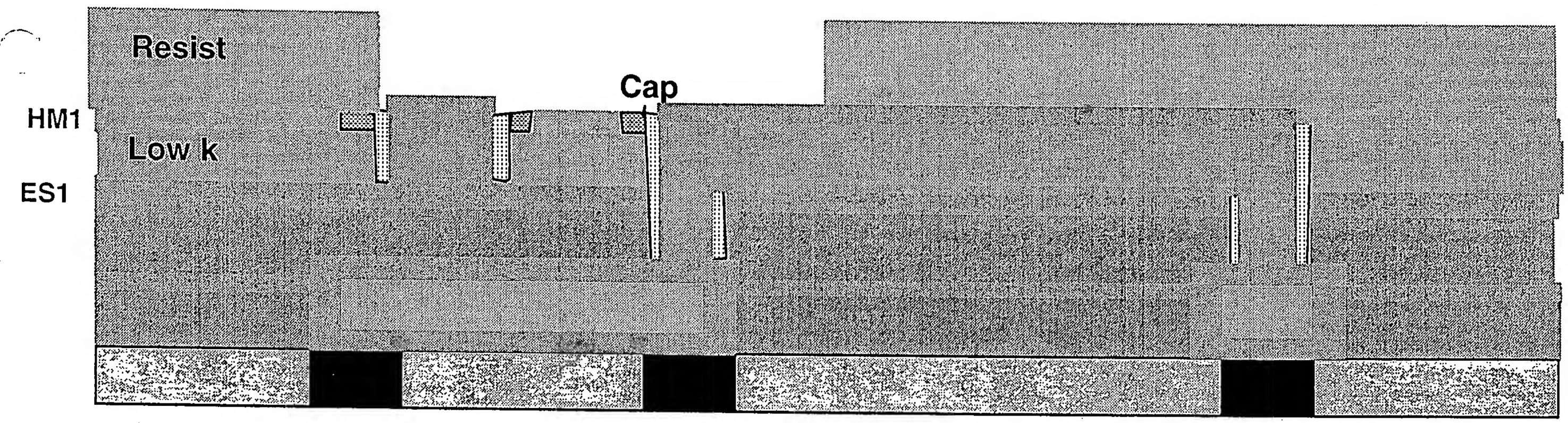


Oxide Spacer Etch & Cap Open

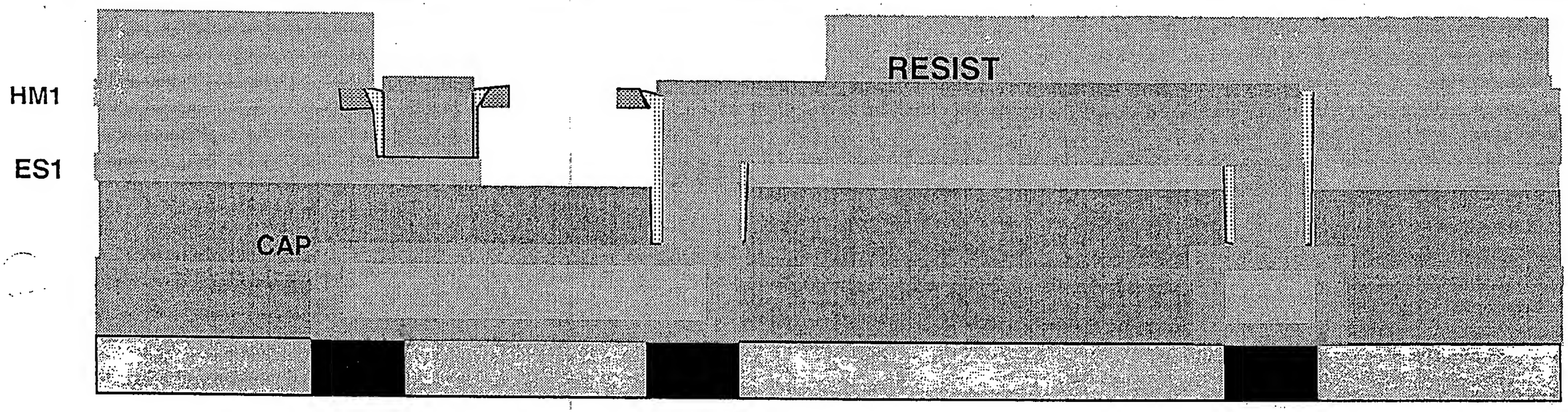
Cu Deposition



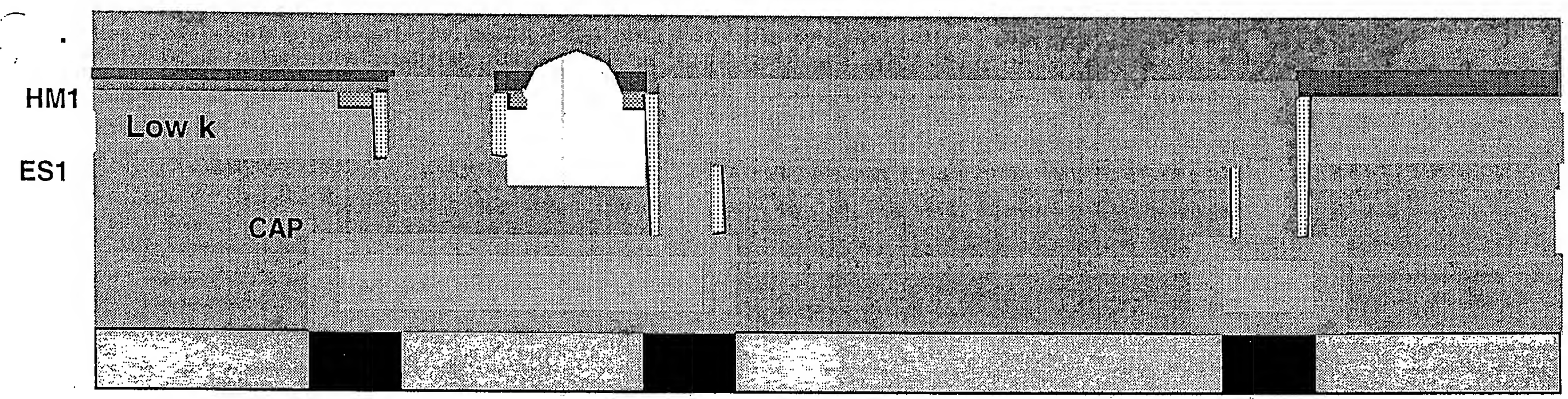
Liner/Seed layer,Cu Deposition- Chem Mech Polish



Deposition of Capping Layer on Cu & Resist Block Mask to expose minimum space areas



Etch SiC HM1, Extract Low k & Etch SiC in Min.Space Areas



Conformal Insulator Deposition - FSG to form Airgap